ABSTRACT

An evaluation TEG for evaluating a semiconductor device including an SOI structure and a LOCOS having a birdbeak portion comprises two electrodes 10 and 20 having different electrode widths sufficiently large to disregard the length of the LOCOS birdbeak portion and an electrode 30 having an extremely small width substantially equal to the length of the birdbeak portion. All the electrode have the same length and are connected to test pads 10a, 20a, and 30a, respectively. The capacitance of a parasitic transistor is easily extracted by using the evaluation TEG and the evaluation of parameters causing the hump characteristics is become possible.